30 GHz GaAs MONOLITHIC LOW NOISE AMPLIFER-ANTENNAS

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ABSTRACT

This paper describes the design and performance of 30 GHz low noise amplifiers (LNAs) integrated with slot antennas on GaAs monolithic microwave integrated circuits (MMICs). Various designs are compared, showing the tradeoffs between achievable noise figure, gain and overall chip size. The smallest chip size, measuring 8.6 mm^2, would provide a 2.1 dB noise figure with 9.5 dB associated gain.

1. INTRODUCTION

The use of monolithic microwave and millimeter-wave integrated circuits and antennas has grown significantly over the last few years [1,2]. Behind this growth is the proliferation of commercial wireless applications at millimetric frequencies (personal communications systems, wireless LANs, etc.) where bandwidth is plentiful. The advantage of such designs is that their MMIC format can lead to entire receiver subsystems on a chip, providing better reproducibility and lower circuit losses than their hybrid counterparts.

A monolithically integrated transmit amplifier-antenna consisting of a slot radiator and a pseudomorphic HEMT device, as shown in Figure 1, has been previously developed by the author [3]. The structure is very compact and exhibits low loss as a result of the elimination of matching circuitry between the HEMT and the slot antenna. This is accomplished by ensuring that the device and slot impedances are a conjugate match.

A similar approach is now followed to develop a 30 GHz low noise amplifier-antenna. Given a certain foundry process, there is freedom to choose the device size and bias current from a range of values, but with little a priori knowledge of how these choices will affect the gain, noise figure or overall circuit realizability. This paper outlines the design procedure for such active antenna structures and points out the tradeoffs between obtainable performance and overall chip size. The unique contributions made here are 1) the achievement of a monolithic low noise receiver front end element suitable for array applications, and 2) the demonstration of slot geometry optimization (size, feed location) to reduce the chip size without affecting noise performance.

2. DESIGN

This being a class of active antenna in which the radiator and circuit interact only through the transmission line, the complete modeling of the amplifier/antenna structure first requires determination of the slot impedance for subsequent use with the device equivalent circuit [4]. Although commercially available EM tools could be used to obtain the slot impedance, a tailor-made integral equation/moment method solver was employed which requires less computation time and allows antenna synthesis [3]. Thus, upon specification of a desired antenna impedance, the program finds a slot length (L), width (W) and feedpoint location (D) yielding this result, provided such a combination exists.

With reference to Figure 2, the remaining steps for designing the integrated LNA/antenna may be summarized as follows (biasing circuitry omitted).

The slot impedance Z_S is the effective generator impedance presented to the device input, and is therefore chosen to provide minimum noise (F_{min}) operation of the device at a given bias current. Thus $\Gamma_s = (Z_S-Z_O)/(Z_S+Z_O)$ is made equal to the device Γ_{opt}, where Γ_{opt} corresponds to F_{min}.

Slot geometry:

Using the previously described synthesis tool, slot dimensions L, W and D are found to produce Z_S. Caution is exercised when L is greater than a half-wavelength as single lobe radiation may not be obtained for off-centre feedpoints [5].

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Output matching:

Maximum gain is desired, so the output impedance transformation network is designed to conjugately match the load to the device. Stability of the complete amplifier is also verified.

Determination of overall gain:

The slot may be treated as a magnetic dipole having a certain directivity and effective area. Thus, for a constant incident power density P_{INC}, the open circuit voltage appearing across the slot will depend on its dimensions. Circuit theory is then employed to calculate the power P_R delivered to the device and finally that to the load, P_{OUT}. The resulting gain expression P_{OUT}/P_{INC} is used here as a basis for comparing the performance of different active antennas.

3. SIMULATED AND MEASURED PERFORMANCE

Noise parameter and small-signal equivalent circuit data were available for the MA/Com 0.2 μm AlGaAs P-HEMT process at drain currents of 10 mA and 15 mA (one gatewidth value only). For these two bias points, several 30 GHz LNA/antenna designs were conducted. The resulting configurations and performance are summarized in Table 1, while the fabricated circuit for the second entry is shown in Figure 3 (DC biasing done off-chip).

At 15 mA drain current, three different slot geometries are given which provide the same impedance Z_S. It is seen that off-centre feeding ($D/L < 0.5$) allows a substantial shortening of the slot length and hence chip area. This advantage is to be weighed against the corresponding loss of gain which results from the lower directivity of short slots. The three designs have the same noise figure since the slot impedance is unchanged. An interesting point emerges from the active antenna realized at 10 mA bias current. Here the noise figure decreases as expected, but an increase in gain is still observed (despite a lower maximum available gain) because the slot now presents a low-noise impedance closer to the value required for maximum gain. All four circuits provide stable operation.

Measurements to date, shown in Figure 4, indicate that good impedance matching has been achieved at 30 GHz for several samples of the active antenna (Fig. 4a). These results, along with the single-lobe E-plane pattern presented in Fig. 4b for an identical passive antenna on an extended 5 cm circular ground plane, are sufficient to confirm the gain and noise values given in Table 1. Complete LNA/antenna gain, noise figure and radiation measurements are now possible.

4. CONCLUSION

The design of millimeter-wave integrated LNA/slot-antennas has been carried out at 30 GHz. A judicious choice of slot geometry and device bias current can lead to receiver front-ends exhibiting high gain and low noise while minimizing chip area and DC power consumption. To the author's knowledge, this is the only design which exploits the slot geometry in such a way as to avoid matching networks between device and radiator.

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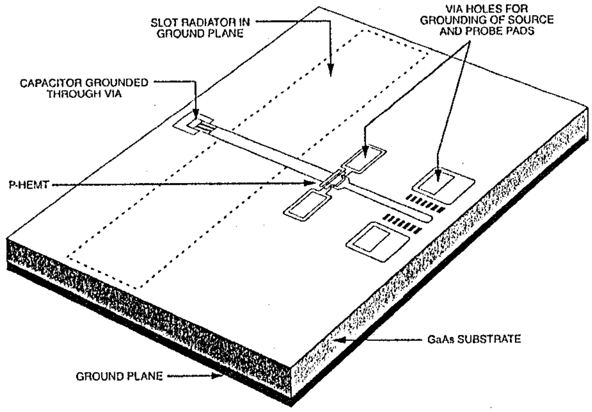

Figure 1. Monolithically integrated amplifier/slot antenna.

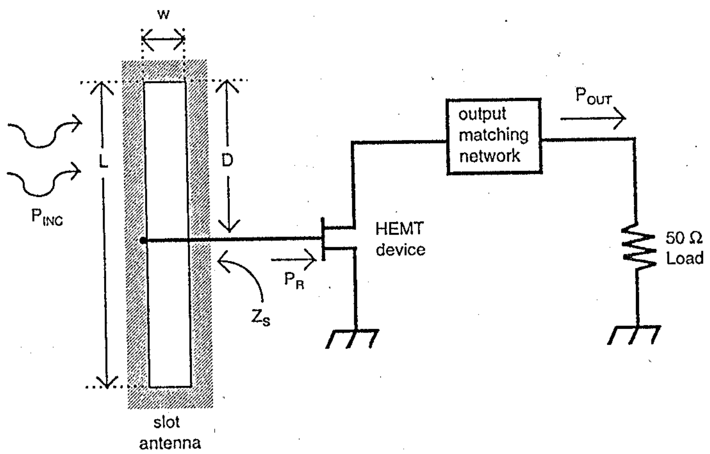

Figure 2. Elements included in the design of an integrated LNA/antenna.

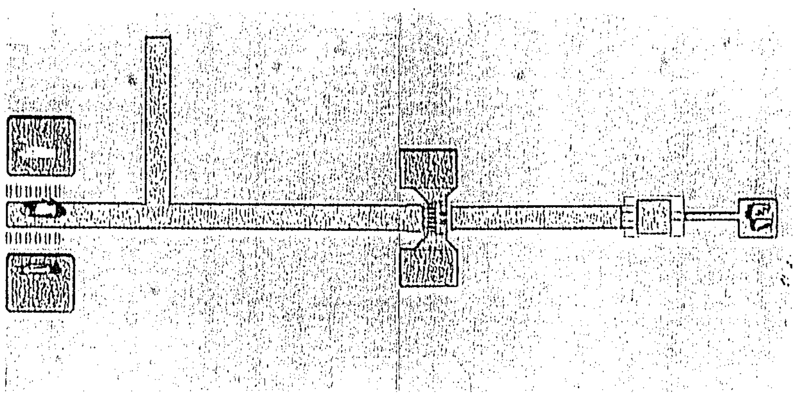

Figure 3. Fabricated MMIC 30 GHz LNA/antenna (slot in underlying ground plane).

Table 1. Four possible 30 GHz LNA/antenna configurations.

Drain Current (mA)	Zs (Ohms)	Slot L(mm)	Slot W(mm)	D/L	Directivity (dB)	Gain (dB)	Noise Figure (dB)	Chip size (mm^2)
15	15 + j8	3.5	0.21	0.25	2.5	9.5	2.1	8.6
15	15 + j8	4.2	0.30	0.4	3.4	10.4	2.1	10.1
15	15 + j8	4.7	0.33	0.5	3.8	10.8	2.1	11.2
10	9 + j13	4.2	0.28	0.35	2.4	11.4	1.9	10.1

Note: Gain is defined as P_{OUT}/P_{INC}

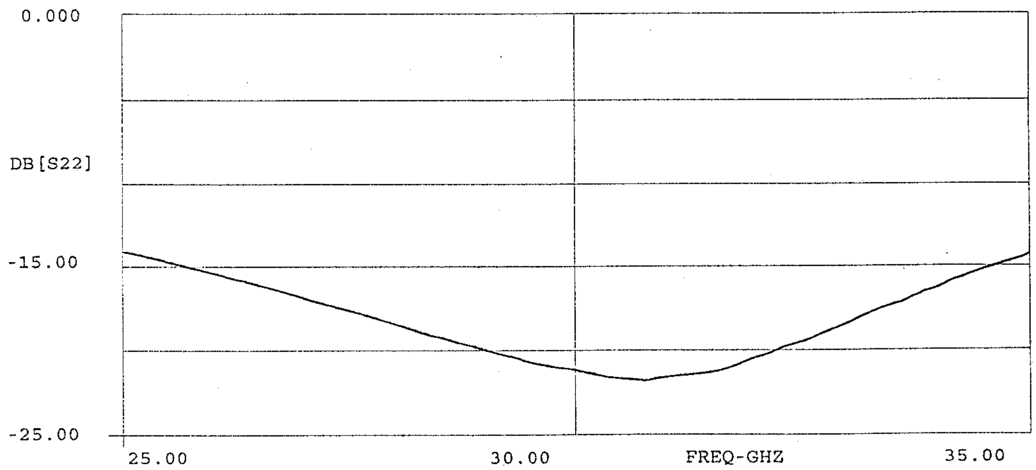

Figure 4a. Measured output impedance of integrated antenna.

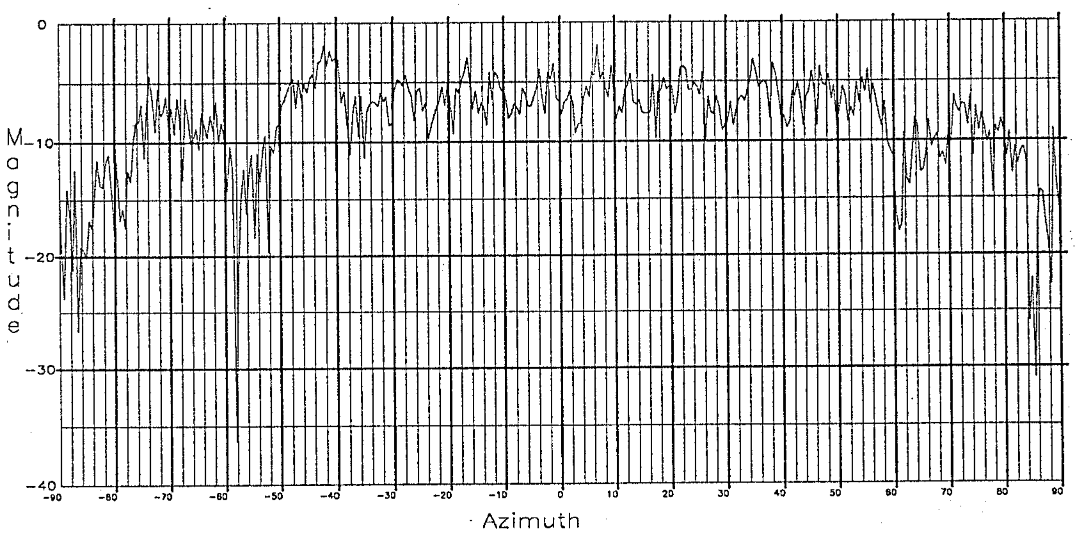

Figure 4b. Measured E-plane pattern of identical passive slot antenna.